

Notification reference number: 4030822057

Mailing number: 053563

Mailing date: April 21, 1998 Page 1 out of 2

Notice of Rejection

Patent Application No.: H3-058520

Date: April 16, 1998

Examiner: Yoji Miyoshi No. 9564 5E00

Patent Attorney(s): Tomoyuki Takimoto and one more attorney

Rule(s) applied for Rejection: Rule 29, section 2

The above-identified application has been rejected from the reason cited below. The applicant is allowed to file a response to this communication within 60 days from the mailing date of this Notice of Rejection.

Reason for Rejection

A patent may not be obtained for the invention set forth in the claim(s) under the Rule 29, section 2, which says from the invention(s) disclosed in the domestic and/or foreign publication(s) identified below, the subject matter sought to be patented would have been obvious to a person having ordinary skill in the art to which said subject matter pertains before the time the invention was made.

Remarks (For the details of Reference, refer to the Notice of Reference Cited)

- Rejected Claim(s): Claims 1 to 18
- Reference: Document number 1 to 3
- Detail: The References 1 and 2 disclose the structure having a block which continuously passes a current and a block which cuts the power at the time of intact. The invention set forth in the claim(s) only applies the strong dielectric constant liquid crystal cited in the Reference 3, for example, to the display device disclosed in the References 1 and 2.

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Mailing number: 053563

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- Rejected claim(s): Claims 19 to 21
- Reference: Document number 1 and 2

There have been no specific reasons to reject the claims unlisted in this Notice of Rejection. However, once such a reason is found, Notice of Rejection can be issued in the future.

Notice of Reference Cited

1. Patent Laid-Open # H2-173818
2. Patent Laid-Open # S61-288725
3. Patent Laid-Open # S64-092826

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拒絶理由通知書



特許出願の番号 平成 3年 特許願 第058520号
起案日 平成10年 4月16日
特許庁審査官 三好 洋治 9564 5E00
特許出願人代理人 滝本 智之 (外 1名) 殿
適用条文 第29条第2項

この出願は、次の理由によって拒絶をすべきものである。これについて意見があれば、この通知書の発送の日から60日以内に意見書を提出されたい。

理 由

この出願の下記の請求項に係る発明は、その出願前日本国内又は外国において頒布された下記の刊行物に記載された発明に基いて、その出願前にその発明の属する技術の分野における通常の知識を有する者が容易に発明をすることができたものであるから、特許法第29条第2項の規定により特許を受けることができない。

記 (引用文献等については引用文献等一覧参照)

- ・請求項： 1～18
- ・引用文献： 1～3
- ・備考：

引用文献1、2には、常時通電するブロックと未使用時には電源を遮断するブロックからなる構成が記載されている。

請求項の発明は、引用文献1、2の表示装置に例えば引用文献3のような強誘電液晶を適用したものにすぎない。

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- ・請求項： 19～21
- ・引用文献： 1～2

この拒絶理由通知書で指摘した請求項以外の請求項に係る発明については、現時点では、拒絶の理由を発見しない。拒絶の理由が新たに発見された場合には拒絶の理由が通知される。

引 用 文 献 等 一 覧

1. 特開平02-178818号公報
2. 特開昭61-288725号公報
3. 特開昭64-092826号公報

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10月12日(木) 11時18分 宛先: 7011120277 250

発信: 松下電器産業株式会社 知的財産権センター

R: 980

P: 02/07

Notification reference number: 2032410422

Mailing number: 208789

Mailing date: July 25, 2000 Page 1 out of 2

Notice of Rejection

Patent Application No.: H11-352963

Date: July 14, 2000

Examiner: Sadatsugu Tanaka No. 9741 5E00

Patent Attorney(s): Fumio Iwahashi and two more attorneys

Rule(s) applied for Rejection: Rule 29, section 2

The above-identified application has been rejected from the reason cited below. The applicant is allowed to file a response to this communication within 60 days from the mailing date of this Notice of Rejection.

Reason for Rejection

A patent may not be obtained for the invention set forth in the claim(s) under the Rule 29, section 2, which says from the invention(s) disclosed in the domestic and/or foreign publication(s) identified below, the subject matter sought to be patented would have been obvious to a person having ordinary skill in the art to which said subject matter pertains before the time the invention was made.

Remarks (For the details of Reference, refer to the Notice of Reference Cited)

- Rejected Claim(s): Claims 1 and 2
- Reference: Document number 1 and 2
- Detail: The Reference 1 discloses an electronic equipment having CPU for rather complicated processing and LSI for regular processing wherein outputting clocks to said CPU is started when information is inputted to said equipment. The Reference 2 also discloses the same invention.

7/14/00
J. I. H.

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10月12日(木) 11時18分 宛先: 7011120272 250

発信: 松下電器産業 知的財産センター

R: 930

P: 03/07

Mailing number: 208789

Mailing date: July 25, 2000 Page 2 out of 2

Notice of Reference Cited

1. Patent Laid-Open # H1-293742
2. Patent Laid-Open # S57-92932

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Notification reference number: 2032410424

Mailing number: 326066

Mailing date: November 14, 2000 Page 1 out of 3

Notice of Rejection

Patent Application No.: 2000-002187

Drafting Date: November 2, 2000

Examiner: Nobuyuki Ishida

No. 9469 5E00

Patent Attorney(s): Fumio Iwahashi and two more attorneys

Rule(s) applied for Rejection: Rule 29, Section 2

The above-identified application has been rejected from the reason cited below. The applicant is allowed to file a response to this communication within 60 days from the mailing date of this Notice of Rejection.

Reason of Rejection

A patent may not be obtained for the invention set forth in the claim(s) under the Rule 29, section 2, which says from the invention(s) disclosed in the domestic and/or foreign publication(s) identified below, the subject matter sought to be patented would have been obvious to a person having ordinary skill in the art to which said subject matter pertains before the time the invention was made.

Remarks (For the details of Reference, refer to the Notice of Reference Cited)

- Rejected Claim(s): Claims 1 to 10
- Reference: Document numbers 1,2 and 3
- Detail: Document 1 discloses an information processing apparatus having an entire system mode to provide system clocks to a first circuit group and a second circuit group, a display mode to have said first circuit group out of use and keep said second circuit group in use, a process mode to keep said first circuit group in use and to have said second circuit group out of use, and an off mode to disconnect both said first and second circuit groups, in which employs a controller of power consumption which is used in order to switch said three modes by detecting inputted information from a key board with an independent circuit group. (See fig. 3 and 4)

The structure for providing clock signals of necessary frequency required in order to maintain data in a register at a pause mode for saving power consumption has been well known as

Page 2 out of 3

disclosed in Document 2. (See fig. 6) Also the structure to generate and provide an allotted clock signal to every functional circuit has been disclosed in Document 3. (See fig. 2, page 3 upper left column) It would be possible for a person with ordinary skill in the art to predict the invention cited in the claims 1 to 10 by having the well-known structure disclosed in the Reference 2 over the information processing apparatus of the Document 1.

- Rejected Claim(s): Claims 1 to 10
- Reference: Document numbers 1,2, 3, 4, 5, 6, 7 and 8
- Detail: Document 4 discloses an information processing apparatus having a key-in time out detecting circuit to have a microprocessor started with a key-in interrupt signal from a keyboard control circuit to detect a key-in from a keyboard and to have the microprocessor stopped with a key-in time out signal.

Document 5 discloses an information processing apparatus having a control circuit to have a microcomputer started with a key-in interrupt signal peripheral circuits and to have it stopped with a

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pause signal from the microcomputer.

Document 6 discloses an information processing apparatus having a cut-in controller to send out a cut-in signal received from functional peripheral circuits to a sleep clock controller which has CPU started with a cut-in demand and CPU stopped when the CPU has no task to conduct.

Document 7 discloses an information processing apparatus having CPU to stop its operation by HALT instruction when there is no key input and to start its operation with an interrupt request from outside.

The structure to provide a microprocessor and an information processing apparatus having function circuits around with a clock signal of an appropriate frequency is well-known, as seen in Documents 3 and 8. It would be possible for a person with ordinary skill in the art to predict the invention cited in the claims 1 to 10 by having the well-known structure disclosed in the 3 and 8 Documents over the information processing apparatus of Documents 1, 4, 5, 6 and 7.

There have been no specific reasons to reject the claims unlisted in this Notice of Rejection. However, once such a reason is found in the future, another Notice of Rejection will be issued.

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Notice of Reference Cited

1. Patent laid-open # S56-132654
2. Microfilm disclosed in Utility model application # S58-79888 (Utility model laid-open # S59-20352)
3. Patent laid-open # H1-228006
4. Patent laid-open # S60-241116
5. Patent laid-open # H2-82306
6. Patent laid-open # S62-169219
7. Patent laid-open # H1-175015
8. Patent laid-open # S63-53626

Record of the prior art search result

- Searched area: IPC 7, G06F 1/04 301
G06F 1/32
- Prior Art Documents: Patent laid-open # H1-251120
Patent laid-open # H1-113818
Patent laid-open # S63-157253
Patent laid-open # S61-24353

The above references are not applied for the reasons for the rejection.

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Notification reference number: 2032410427

Mailing number: 326065

Mailing date: November 14, 2000 Page 1 out of 3

Notice of Rejection

Patent Application No.: 2000-002186

Drafting Date: November 2, 2000

Examiner: Nobuyuki Ishida

No. 9469 5E00

Patent Attorney(s): Fumio Iwahashi and two more attorneys

Rule(s) applied for Rejection: Rule 29, Section 2

The above-identified application has been rejected from the reason cited below. The applicant is allowed to file a response to this communication within 60 days from the mailing date of this Notice of Rejection.

Reason of Rejection

A patent may not be obtained for the invention set forth in the claim(s) under the Rule 29, section 2, which says from the invention(s) disclosed in the domestic and/or foreign publication(s) identified below, the subject matter sought to be patented would have been obvious to a person having ordinary skill in the art to which said subject matter pertains before the time the invention was made.

Remarks (For the details of Reference, refer to the Notice of Reference Cited)

- Rejected Claim(s): Claims 1 to 9
- Reference: Document numbers 1,2 and 3
- Detail: Document 1 discloses an information processing apparatus having an entire system mode to provide system clocks to a first circuit group and a second circuit group, a display mode to have said first circuit group out of use and keep said second circuit group in use, a process mode to keep said first circuit group in use and to have said second circuit group out of use, and an off mode to disconnect both said first and second circuit groups, in which employs a controller of power consumption which is used in order to switch said three modes by detecting inputted information from a key board with an independent circuit group. (See fig. 3 and 4)

The structure for providing clock signals of necessary frequency required in order to maintain data in a register at a pause mode for saving power consumption has been well known as

Page 2 out of 3

disclosed in Document 2. (See fig. 6) Also the structure to generate and provide an allotted clock signal to every functional circuit has been disclosed in Document 3. (See fig. 2, page 3 upper left column) It would be possible for a person with ordinary skill in the art to predict the invention cited in the claims 1 to 9 by having the well-known structure disclosed in the Reference 2 over the information processing apparatus of the Document 1.

- Rejected Claim(s): Claims 1 to 9
- Reference: Document numbers 1,2, 3, 4, 5, 6, 7 and 8
- Detail: Document 4 discloses an information processing apparatus having a key-in time out detecting circuit to have a microprocessor started with a key-in interrupt signal from a keyboard and to have the microprocessor stopped with a key-in time out signal.

Document 5 discloses an information processing apparatus having a control circuit to have a microcomputer started with a key-in interrupt signal from peripheral circuits and to have it stopped with

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a pause signal from the microcomputer.

Document 6 discloses an information processing apparatus having a sleep clock controller to have CPU started with an interrupt request and CPU stopped when the CPU has no task to execute.

Document 7 discloses an information processing apparatus having CPU to stop its operation by HALT instruction when there is no key input and to start its operation with an interrupt request from outside.

In an information processing apparatus having a microprocessor and a functional peripheral circuit, the structure to provide the microprocessor and the functional peripheral circuit with a clock signal of an appropriate frequency is well-known, as seen in Documents 3 and 8. It would be possible for a person with ordinary skill in the art to predict the invention cited in the claims 1 to 9 by having the well-known structure disclosed in the 3 and 8 Documents over the information processing apparatus of Documents 1, 4, 5, 6 and 7.

There have been no specific reasons to reject the claims unlisted in this Notice of Rejection. However, once such a reason is found in the future, another Notice of Rejection will be issued.

Page 3 out of 3

Notice of Reference Cited

1. Patent laid-open # S56-132654
2. Microfilm disclosed in Utility model application # S58-79888 (Utility model laid-open # S59-20352)
3. Patent laid-open # H1-228006
4. Patent laid-open # S60-241116
5. Patent laid-open # H2-82306
6. Patent laid-open # S62-169219
7. Patent laid-open # H1-175015
8. Patent laid-open # S63-53626

Record of the prior art search result

- Searched area: IPC 7, G06F 1/04 301
G06F 1/32
- Prior Art Documents: Patent laid-open # H1-251120
Patent laid-open # H1-113818
Patent laid-open # S63-157253
Patent laid-open # S61-24353

The above references are not applied for the reasons for the rejection.

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Type of document: Decision of Rejection

Mailing number: 318830

Patent H11-352963(.00.00)

Mailing date: November 7, 2000 Page 1 out of 2

Decision of Rejection

Patent Application No.: H11-352963

Drafting Date: October 30, 2000

Examiner: Sadatsugu Tanaka

No. 9741 5E00

Title of the invention: Information Processing Apparatus and Method for Controlling Its Electricity

Applicant: Matsushita Electric Industrial Co., Ltd.

Patent Attorney(s): Fumio Iwahashi and two more attorneys

Decision of Rejection is issued to the above-identified application from the reason cited in the Notice of Rejection dated July 14, 2000.

Opinion and Amendment filed by the applicant were accepted and examined its contents. However enough reasons to overcome the reasons of rejection could not been found.

Remarks

The applicant argued the following two points in Opinion:

1) The invention set forth in this application is different from the invention disclosed in Document 1 because the speed of the operating clock of the second processing unit is faster than the one of the operating clock of the first processing unit in the present invention.

2) The invention set forth in this application is different from the invention disclosed in Document 1 because the second processing unit of the present invention possesses a main processing unit and a starting unit, in which the starting unit keeps its operation and stops the main processing unit when an input is not sent from outside to an information input unit, and the starting unit starts the main processing unit when the information input unit receives an input while the main unit stops its operation.

However, after considering the filed argument points, the following statement is found to deny the argument point 1 in Document 1, page 2, from line 8 to line 12 of the lower right column:

...as explained, main CPU 1 and its memory system are operated at a high-speed clock. Since these units are not operated frequently in an intermittent manner, though the units consume rather high energy, the total power consumption of the entire mobile telephone can be tremendously reduced.

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On the argument point 2: It is obvious for the to a person having ordinary skill in the art to which said subject matter pertains that a main CPU constantly operates no matter if there is any input from outside, and has a structure to watch an interrupt request signal from LSI, and the structure determines if processing at the main CPU is stopped or started by applying the teaching in Document 1, in which the disclosed LSI applies or stops a master clock for a main CPU, and generates an interrupt request signal when a receiving signal is inputted, and the main CPU starts its operation with said interrupt request signal.

Therefore the argument filed by the applicant is not applicable to overcome the rejection.

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Notification reference number: 2032410427

Mailing number: 204414

Mailing date: July 18, 2000 Page 1 out of 2

Notice of Rejection

Patent Application No.: 2000-002186

Date: July 11, 2000

Examiner: Nobuyuki Ishida No. 9469 5E00

Patent Attorney(s): Fumio Iwahashi and two more attorneys

Rule(s) applied for Rejection: Rule 29, section 2

The above-identified application has been rejected from the reason cited below. The applicant is allowed to file a response to this communication within 60 days from the mailing date of this Notice of Rejection.

Reason for Rejection

A patent may not be obtained for the invention set forth in the claim(s) under the Rule 29, section 2, which says from the invention(s) disclosed in the domestic and/or foreign publication(s) identified below, the subject matter sought to be patented would have been obvious to a person having ordinary skill in the art to which said subject matter pertains before the time the invention was made.

Remarks (For the details of Reference, refer to the Notice of Reference Cited)

- Rejected Claim(s): Claims 1 to 4
- Reference: Document number 1 and 2
- Detail: The Reference 1 discloses an information processing apparatus having an entire system mode to provide system clocks to a first circuit group and a second circuit group, a display mode to have said first circuit group out of use and keep said second circuit group in use, a processing exclusive mode to keep said first circuit group in use and have said second circuit group out of use, and an off mode to have both said first and second circuit groups unavailable, in which employs a controller for power consumption which is used in order to control electricity in switching among said four modes by detecting inputted information from a key board with an independent circuit group. (See fig. 3 and 4)

The structure for providing clock signals of frequency needed, at least, in order to maintain data in a register has been well known as disclosed in the reference 2. (See fig. 6) It would be possible for a person with ordinary skill in the art to predict the invention cited in the claims 1 to 4 by applying the

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Mailing number: 204414

Mailing date: July 18, 2000 Page 2 out of 2

well-known structure disclosed in the Reference 2 over the information processing apparatus of the Reference 1.

There have been no specific reasons to reject the claims unlisted in this Notice of Rejection. However, once such a reason is found, Notice of Rejection can be issued in the future.

Notice of Reference Cited

1. Patent Application Laid-Open # S56-132654
2. The micro-film disclosed in Utility Model Appl. # S58-79888 (Utility Model Laid Open # S59-20352)

Record of the prior art search result

- Area of Search: IPC 7 G06F 1/04 301
G06F 1/32

- Searched References: Patent Laid-Open # H2-82306
Patent Laid-Open # H2-66664
Patent Laid-Open # S63-157253
Patent Laid-Open # S61-288725
Patent Laid-Open # S61-43344
Patent Laid-Open # S55-92961

The above references are not applied for the reasons for the rejection.

Notification reference number: 2032410424

Mailing number: 204415

Mailing date: July 18, 2000 Page 1 out of 2

Notice of Rejection

Patent Application No.: 2000-002187

Date: July 11, 2000

Examiner: Nobuyuki Ishida No. 9469 5E00

Patent Attorney(s): Fumio Iwahashi and two more attorneys

Rule(s) applied for Rejection: Rule 29, section 2

The above-identified application has been rejected from the reason cited below. The applicant is allowed to file a response to this communication within 60 days from the mailing date of this Notice of Rejection.

Reason for Rejection

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Remarks (For the details of Reference, refer to the Notice of Reference Cited)

- Rejected Claim(s): Claims 1 to 3
- Reference: Document number 1 and 2
- Detail: The Reference 1 discloses an information processing apparatus having an entire system mode to provide system clocks to a first circuit group and a second circuit group, a display mode to have said first circuit group out of use and keep said second circuit group in use, a processing exclusive mode to keep said first circuit group in use and have said second circuit group out of use, and an off mode to have both said first and second circuit groups unavailable, in which employs a controller for power consumption which is used in order to control electricity in switching among said four modes by detecting inputted information from a key board with an independent circuit group. (See fig. 3 and 4)

The structure for providing clock signals of frequency needed, at least, in order to maintain data in a register has been well known as disclosed in the reference 2. (See fig. 6) It would be possible for a person with ordinary skill in the art to predict the invention cited in the claims 1 to 4 by applying the

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Mailing number: 204415

Mailing date: July 18, 2000 Page 2 out of 2

well-known structure disclosed in the Reference 2 over the information processing apparatus of the Reference 1.

There have been no specific reasons to reject the claims unlisted in this Notice of Rejection. However, once such a reason is found, Notice of Rejection can be issued in the future.

Notice of Reference Cited

3. Patent Application Laid-Open # 56-132654
 4. The micro-film disclosed in Utility Model Appl. # S58-79388 (Utility Model Laid Open # S59-20352)
-

Record of the prior art search result

- Area of Search: IPC 7 G06F 1/04 301
G06F 1/32
- Searched References: Patent Laid-Open # H2-82306
Patent Laid-Open # H2-66664
Patent Laid-Open # S63-157253
Patent Laid-Open # S61-288725
Patent Laid-Open # S61-43344
Patent Laid-Open # S55-92961

The above references are not applied for the reasons for the rejection.